REMARKS

Claims 1-18 and 34 are pending in the instant application. Claims 1 and 34 are amended herein. No new matter has been added as a result of the amendments made herein.

103 Rejections

Claims 1-18 and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admission of Prior Art (AAPA), in view of Rawlings et al, (U.S. Patent No. 4,156,907). The Applicant has reviewed the cited references and respectfully submit that embodiments of the present invention as are set forth in Claims 1-18 and 34 are neither anticipated nor rendered obvious by AAPA in view of Rawlings et al.

Independent Claim 1

The Examiner is respectfully directed to independent Claim 1 which sets forth that an embodiment of the present invention includes a computer capable of playing real time applications, that comprises:

> ...a processing circuit configured to operate in a first power state, a second power state, and a third power state, said processing circuit consuming less power in said second power state than in said first power state, and said processing circuit consuming less power in said third power state than in said second power state; and a real time subsystem coupled to said processing circuit, said real time subsystem comprising a buffer, said buffer configured to store data and output said data to an output device <u>for playing said real time applications</u> thereby enabling said processing circuit to enter said third power state while said buffer is outputting said data.

Applicant respectfully submits that neither AAPA, Rawlings, nor their combination renders obvious a real time subsystem for playing real time applications and enabling a processing circuit to enter a third power state as is set forth in amended Claim 1.

As expressly disclosed in the Rawlings reference, particularly referring to col. 2, lines 24-33, the field of this invention pertains to data processing equipment which is intended for use with terminal devices. The terminal devices involved are generally employed to convert the data from a humanly readable form into binary digital form. The apparatus disclosed in the Rawlings reference is related to a computer system coupled to a plurality of the terminal devices that converts the data from a humanly readable form into binary form. Moreover, the communication subsystem in the Rawlings reference is used for the routing, monitoring and controlling data messages between a plurality of remote terminals, see col. 3 lines 30-34. Further, referring to col. 4 lines 14-25 and col. 60 lines 8-23, the data communications processor of a subsystem can sense a failure or a halt-load condition of the main host processor, and, during this period, the data which would normally be sent to the main host system would be "tanked" into a disk file memory until such time as the main host system is "on-line" again. It should be understood that the real time applications of the claimed invention, such as audio and video, requires the computer system to be able to respond to any request at any time. However, the communication system of the Rawlings reference, which works until the main host system is on-line again, actually teaches away form the real time application of the claimed invention. Therefore, it is respectfully submitted that Rawlings does not anticipate or render obvious any real time application.

Furthermore, Rawlings does not teach the claimed limitation, "thereby enabling said processing circuit to enter said third power state while said buffer is outputting said data." As mentioned above and referring to col. 4 lines 14-25 and col. 60 lines 8-23, the data communication subsystem includes a mechanism that senses any halt in operation of the main host system. However, Nowhere in the Rawlings's reference is a process or means to enable the main host processor to enter any state shown or suggested as is recited in claim 1. Consequently, the embodiment of the Applicant's invention as set forth in Claim 1 is neither anticipated nor rendered obvious by Rawlings.

Thus, Applicants respectfully submit that the present invention as disclosed in independent Claim 1 is not anticipated by Rawlings taken alone or in combination with Applicant's Admission of Prior Art (AAPA), and is thus in a condition for allowance. In addition, Applicant respectfully submits that Claims 2-5 which depend from independent Claim 1 are also in a condition for allowance as being dependent on an allowable base claim.

Independent Claim 6

The Examiner is respectfully directed to independent Claim 6 which sets forth that an embodiment of the present invention includes a real time subsystem, that comprises:

> ...a buffer configured to store data for use in said real time subsystem enabling a processing circuit of a computer to enter a deep sleep state while said computer is running said real time subsystem.

Regarding independent Claim 6, the Rawlings reference does not disclose or suggest implementing a computer which is able to run a real time subsystem and enable the processing circuit of the computer to enter a deep sleep state. Therefore, it is respectfully

submitted that Rawlings does not render obvious a real time subsystem as presently claimed in Claim 6.

Thus, Applicant respectfully submits that the present invention as disclosed in independent Claim 6 is not anticipated by the Rawlings reference taken alone or in combination with Applicant's Admission of Prior Art (AAPA), and is in condition for allowance. In addition, Applicant respectfully submits that Claim 7 which depends from independent Claim 6 is also in a condition for allowance as being dependent on an allowable base claim.

Independent Claim 8

The Examiner is respectfully directed to independent Claim 8 which sets forth that an embodiment of the present invention includes a method of conserving power in a computer while playing a real time application, that comprises the steps of:

> ...reading a storage medium of data for use in said real time application; processing said data in a processing circuit configured to operate in a first power state, a second power state, and a third power state, said processing circuit consuming less power in said second power state than in said first power state, and said processing circuit consuming less power in said third power state than in said second power state; storing said data in a buffer; outputting said data from said buffer to a real time application output device; and placing said processing circuit in said third power state while said buffer is outputting said stored data.

Regarding independent Claim 8, the Rawlings reference does not disclose or suggest implementing a method which is able to output data to a real time application output device

and place a processing circuit in a third power state as is recited in this claim. Therefore, it is respectfully submitted that Rawlings does not render obvious a method as presently claimed in Claim 8.

Thus, Applicant respectfully submits that the present invention as disclosed in independent Claim 8 is not anticipated by Rawlings taken alone or in combination with Applicant's Admission of Prior Art (AAPA), and is in a condition for allowance. In addition, Applicant respectfully submits that Claims 9-18 which depend from independent Claim 8 are also in a condition for allowance as being dependent on an allowable base claim.

Independent Claim 34

The Examiner is respectfully directed to independent Claim 34 which sets forth that an embodiment of the present invention includes a computer capable of playing real time applications, that comprises:

> ...a processing circuit; an output device coupled to said processing circuit via a bus; and a real time subsystem coupled to said processing circuit via said bus, said real time subsystem comprising a buffer, said buffer configured to store data and output said data to said output device for playing said real time applications thereby enabling said processing circuit to enter a deep sleep state while said buffer is outputting said data.

Regarding independent Claim 34, the Rawlings reference does not disclose or suggest implementing a computer which is able to play a real time application and that enables the processing circuit of the computer to enter a deep sleep state as is recited in this claim. Therefore, it is respectfully submitted that Rawlings does not render obvious a computer as presently set forth in amended Claim 34.

Thus, Applicant respectfully submits that the present invention as disclosed in independent Claim 34 is not anticipated by Rawlings taken alone or in combination with Applicant's Admission of Prior Art (AAPA), and is in condition for allowance.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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